IN THE CLAIMS

Please cancel claims 1-2 and amend claims 4, 8 and 9 as follows:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Currently Amended) An apparatus, comprising:

first, second, and third interfaces each having an input and an output;

an interface controller having a first, second, and third control outputs, and operable to enable any one of said outputs individually;

a first, second, third, fourth, fifth, and sixth [[buffer]] buffers, each of the buffers having an input, an output, and a single control input, and wherein said single control inputs enable and disable the coupling of signals through said buffers, and wherein

said output of said first and second buffers are coupled to said input of said first interface;

said outputs of said third and fourth buffers are coupled to said input of said second interface;

said outputs of said fifth and sixth buffers are coupled to said input of said third interface;

said output of said first interface is coupled to said [[input]] inputs of said fourth and fifth [[buffer]] buffers;

said output of said second interface is coupled to said inputs of said first and sixth buffers;

said output of said third interface is coupled to said inputs of said second and third buffers;

said first control output is coupled to both of said single control inputs of said first and fourth buffers to selectively enable bi-directional interconnection of the first interface and second interface;

said second control output is coupled to both of said single control inputs of said third and sixth buffers to selectively enable bi-directional interconnection of the second interface and third interface, and

said third control output is coupled to both of said single control inputs of said second and fifth buffers to selectively enable bi-directional interconnection of the first interface and third interface.

5. (Previously Presented) The apparatus of Claim 4 including means for disabling said control inputs by setting said outputs of said buffers to a high impedance state, and wherein said interface controller is operable to disable all of said control outputs.

6. (Previously Presented) The apparatus of Claim 4 wherein said interfaces are serial port interfaces.

7. (Original) The apparatus of Claim 6 wherein said serial port interfaces are RS-232 serial port interfaces.

8. (Currently Amended) The apparatus of Claim 6 wherein said output of each said serial port interface is a transmit data output, and said input of each said serial port interface is a receive data input.

9. (Currently Amended) The apparatus of Claim 7 wherein said output of each said serial port interface is a request to send output, and said input of each said serial port interface is a clear to send input.

10. (Original) The apparatus of Claim 4 wherein said interface controller is incorporated into one of said interfaces.

11. (Original) An apparatus, comprising:

a plurality of n interfaces, each having an input and an output;

a plurality of n(n-1) buffers, each having an input, an output, and a control input, and wherein said control inputs enable and disable the coupling of signals through said buffers, respectively;

an interface controller having a plurality of $({}_nC_2)$ control outputs, and operable to enable any one of said plurality of outputs individually, and wherein

said outputs of a unique (n-1) of said plurality of buffers are coupled to said input of each one of said plurality of interfaces;

every one of said outputs of said plurality of interfaces is uniquely coupled to said input of one of said (n-1) plurality of buffers that are coupled to said inputs of every other of said plurality of interfaces, such that said output of every interface is coupled to said input of every other interface through a unique one of said plurality of buffers, and

each one of said plurality of control outputs is coupled to said control inputs of the two of said plurality of buffers that couples a unique pair of the $({}_nC_2)$ combinations of said interface inputs and outputs.

12. (Previously presented) The apparatus of Claim 11 wherein disabling said control inputs includes setting said outputs of said plurality of buffers to a high impedance state, and wherein said interface controller is operable to disable all of said plurality of control outputs.

13. (Original) The apparatus of Claim 11 wherein said plurality of interfaces are serial port interfaces.

14. (Original) The apparatus of Claim 13 wherein said serial port interfaces are RS-232 serial port interfaces.

15. (Original) The apparatus of Claim 13 wherein said output of said serial port interface is a transmit data output, and said input of said serial port interface is a receive data input.

16. (Original) The apparatus of Claim 14 wherein said output of said serial port interface is a request to send output, and said input of said serial port interface is a clear to send input.

17. (Original) The apparatus of Claim 11 wherein said interface controller is incorporated into one of said interfaces.